Baseband Assembly Analog-to-Digital Converter Board

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This article reports on the design and development of an upgraded analog-to-digital converter board for the Baseband Assembly (BBA) of the Deep Space Communications Complex Telemetry Subsystem (DTM).

I. Introduction

The BBA combines and processes baseband signal inputs from up to eight Deep Space Network antennas tracking a single spacecraft. The result is an improved symbol signal-to-noise ratio (SSNR) digital telemetry data output for the Telemetry Subsystem (DTM) [1].

The analog-to-digital converter board (ADB) is used by the Real-Time Combiner (RTC) and Demodulator Synchronizer Assembly (DSA) subsystems of the BBA. The function of the ADB in both subsystems is to digitize an analog baseband telemetry signal for subsequent processing (see Fig. 1).

II. Specifications

The ADB is designed to accommodate the mission-independent range of telemetry data rates, type of modulation, SNR, and signal level. The major elements of the ADB are the automatic gain control (AGC) circuit and the analog-to-digital converter (ADC). For a description of the theory of operation of the AGC and ADC, see the Appendix.

This ADB was designed to meet existing system specifications and to provide added operational capability of real-time, high resolution, AGC level and offset control. The primary specifications are given in Table 1.

III. Functional Description

The ADB consists of two identical signal conversion channels and a Multibus I computer interface (see Fig. 2). The interface group provides the logic for standard Multibus I handshake control, board address detection, and on-board device selection. Each analog-to-digital conversion channel consists of an input filter, a gain-controlled input amplifier, a signal amplifier (ADC driver), an automatic gain control circuit (AGC), and D/A converters for vernier gain and offset control.

Vernier gain and offset in the AGC loop are under CPU control. When the system software senses a need for adjustment of either offset or AGC level, the CPU loads the appropriate D/A with a new digital value to effect the necessary change.

IV. Detailed Description

The control section of the board consists of logic for bus control, board and device address decoding, and data buffering. Bus control logic provides standard Multibus I handshake functions for CPU-to-board data transfer. On-board logic is isolated from the bus with tristate buffers to minimize contamination of analog signals by bus activity.

The two dual D/A converters (DACs) are addressed by an external CPU. Data written to the DACs cannot be read back. Data written to a DAC represents a change in the vernier offset or AGC level. The correctness of the new value can be determined by the system software.

The analog input signal is attenuated by a 30-dB pad and filtered by a 7-pole, 7-MHz (50-ohm) low-pass Butterworth filter. The filtered signal is coupled to a gain-controlled amplifier.

The gain-controlled signal is capacitively coupled (DC isolated) to a high-speed operational amplifier which drives the analog-to-digital converter (ADC). The output of the ADC driver has a fixed offset of approximately −1 volt to center the signal in the midrange of the ADC. The CPU-controlled vernier DC offset is summed with the data signal at the input to the amplifier to provide a more exact control of the offset adjustment.

The ADC is a 20-megasample-per-second, full-parallel (flash) analog-to-digital converter capable of converting up to 7 MHz. The ADC is configured for an 8-bit, false, two's-complement output. A system clock is buffered on board to function as the ADC sampling clock.

The AGC circuit consists of a half-wave rectifying power detector and an integrator. The rectified signal is input to the integrating operational amplifier. The output of the integrator drives the control input to the gain-controlled amplifier, closing the AGC loop. The CPU-controlled vernier AGC level is summed with the feedback voltage at the input to the integrator. Manual level control is possible by a hardware configuration of the board and manual level adjustment.

V. Summary

Prototypes of the ADB were tested in a stand-alone configuration to validate the characteristics of data conversion and control functions. The boards were subsequently installed in the Real-Time Combiner and Demodulator Synchronizer assemblies for system integration. Integration consisted of control software development and system performance evaluation. The results of testing, including system evaluation, showed that the prototypes met or exceeded all initial design criteria (see Fig. 3 and Table 1).

Major considerations in the design of the ADB were reliability and ease of calibration. Reliability was addressed by using mature technology, proven circuit design, and electronic components. Manual preinstallation calibration consists of a single coarse offset adjustment per channel. System calibration is completely under software control.

The ADB uses current multilayer printed circuit board (PCB) technology. The PCB was designed solely on an IBM-AT-based Futurenet CAE system. The personal workstation approach to board design gave direct control of component layout and signal trace routing and eliminated time-consuming interaction with drafting/layout technicians. The CAE-generated photo-plot and drill tape were directly used for fabrication.

Reference

[1] C. D. Bartok, "Performance of the Real-Time Array Signal Combiner During Voyager Mission," *TDA Progress Report 42-63*, vol. March–April 1981, pp. 191–202, June 15, 1981.

Table 1. Analog-to-digital converter board specifications

Parameter	Specification
Sample rate	20-MHz maximum
Resolution	8 bits
Digital output	8 bit, two's complement, TTL
Analog 3-dB bandwidth	500 Hz to 7 MHz
Input signal range	+24 to −24 dBm
CPU-controlled offset	
Range	0.2 volt
Resolution	0.2 volt/4096 = 0.049 millivolt
CPU-controlled AGC output level	
Tunable range	6 dB (0.2 volt to 0.8 volt for square wave)
Resolution	6 dB/4096 = 0.00146 dB (factor of 1.00033735)
Input impedance	50 ± 5 ohms

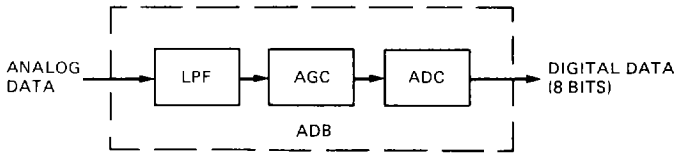

Fig. 1. Analog-to-digital converter board simplified functional diagram

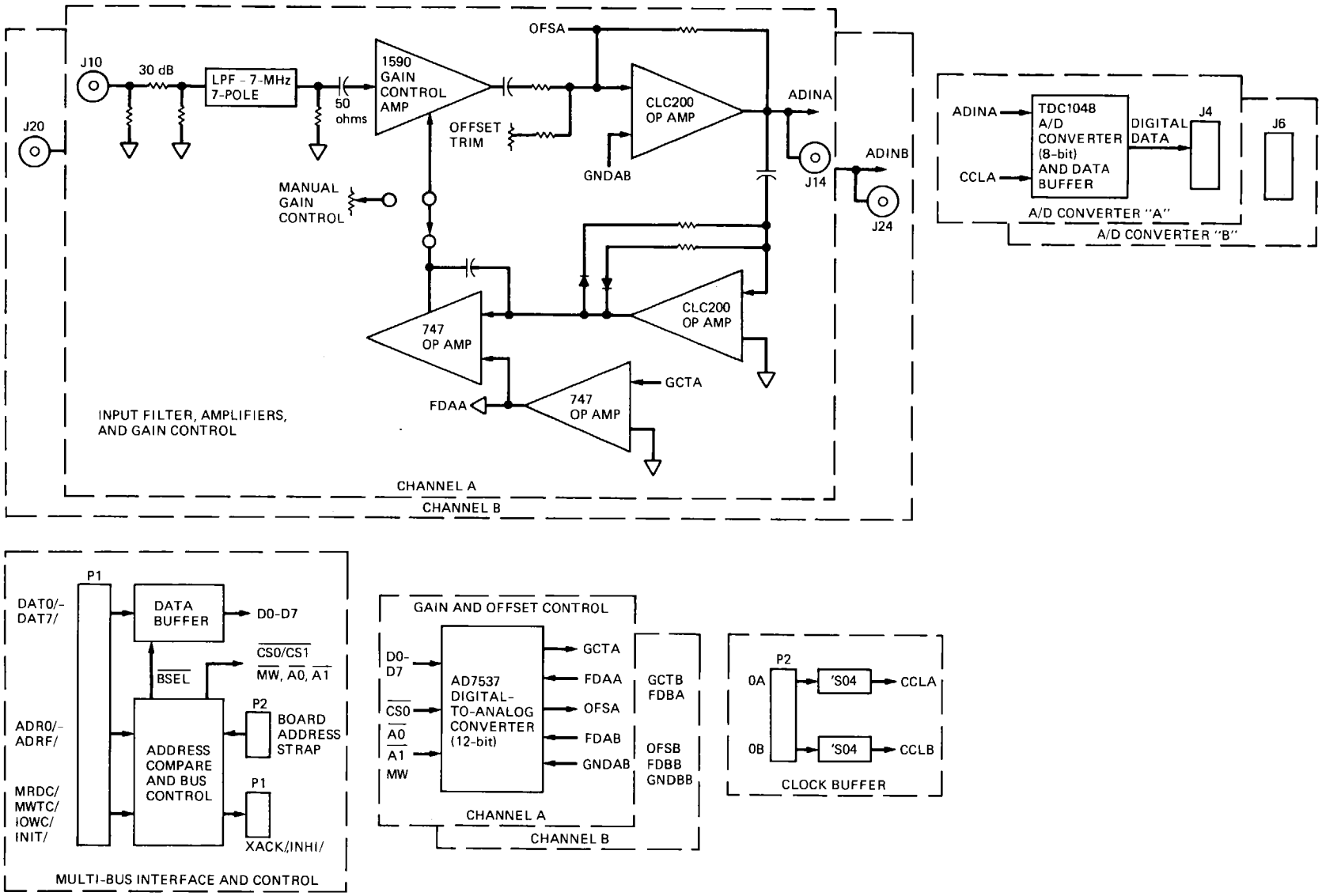

Fig. 2. Analog-to-digital converter board block diagram

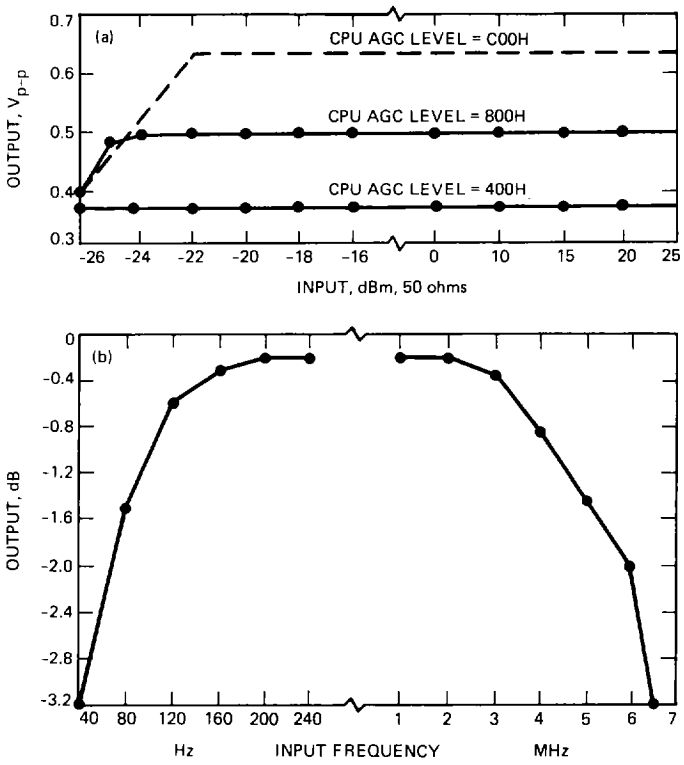

Fig. 3. AGC (a) range and (b) frequency response

Appendix

AGC/ADC Description

The purpose of the automatic gain control (AGC) is to set the signal level so that it is properly scaled and centered in the range of the analog-to-digital converter.

Signal-level detection is performed by a half-wave rectifier. In order to accommodate the full range of symbol SNRs, the input/output levels were set as shown in Table A-1.

I. ADC Characteristics

(8-bit, two's complement, 7-MHz BW, 20 msps)

The full ADC input range is $\pm 128 = \pm 3.19\sigma$ units.

The symbol SNR, R is related to the per-sample SNR, R_{rf}, by

$$R_{rf} = \frac{R \times r_{sy}}{2B} = \frac{S}{2N_0 B} = \frac{\mu_{rf}^2}{2\sigma_{rf}^2}$$

The linear rectifier output has an average value:

$$V_{agc} = \frac{1}{2\sigma\sqrt{2\pi}} \int_0^\infty V e^{-1/2(V-\mu/\sigma)^2}\, dV + \frac{1}{2\sigma\sqrt{2\pi}}$$

$$\times \int_0^\infty V e^{-1/2(V+\mu/\sigma)^2}\, dV$$

$$= \frac{\mu_{rf}}{2}\left[P\left(\sqrt{2R_{rf}}\right) - P\left(-\sqrt{2R_{rf}}\right) + \frac{e^{-R_{rf}}}{\sqrt{\pi R_{rf}}}\right]$$

$$= \frac{\mu_{rf}}{2}\left[P\left(\sqrt{2R_{rf}}\right) - P\left(-\sqrt{2R_{rf}}\right)\right] + \frac{\sigma_{rf}}{\sqrt{2\pi}} e^{-R_{rf}}$$

Thus, the mean sample voltage for any SNR is given by:

$$\mu_{rf} = \frac{2V_{agc}}{\left[P\left(\sqrt{2R_{rf}}\right) - P\left(-\sqrt{2R_{rf}}\right) + \frac{e^{-R_{rf}}}{\sqrt{\pi R_{rf}}}\right]}$$

II. AGC Output Level

For a square-wave input without noise (pure signal), the AGC output is set to –1 V center, 0.5 V peak to peak. In ADC units, this is:

$$V_{agc} = \frac{\mu_{sq}}{2} = 16 \Rightarrow \mu_{sq} = 2V_{agc} = 32 = -1 \pm 0.25 \text{ V}$$

For a noiseless sine wave, we denote the peak values by $\pm\mu_{sin}$ and

$$V_{agc} = 16 = \frac{\mu_{sin}}{\pi} \Rightarrow \mu_{sin} = \pi V_{agc} = 50.3$$

$$= -1 \pm 0.393 \text{ volts p-p}$$

For pure gaussian noise, we have for the average output of the half-wave rectifier:

$$V_{agc} = 16 = \frac{1}{\sigma\sqrt{2\pi}} \int_0^\infty V e^{-V^2/2\sigma^2}\, dV = \frac{\sigma}{\sqrt{2\pi}}$$

or

$$\sigma = \sqrt{2\pi}\, V_{agc} = 40.1 \text{ (rms noise level)}$$

This corresponds to σ = rms noise voltage = 40.1/128 = 0.313 volt into 50-ohm noise power = $\sigma^2/50$ = 1.963 mW = 2.93 dBm.

Table A-1. ADC input/output levels

Input level, V	Output code		
	Hex	Decimal	
−0.008	7FH	127	
−0.750	20H	32	μ_{sq}*
−0.096	D1H	1	
−1.004	00H	0	−1 V = center range
−1.012	FFH	−1	
−0.250	E0H	−32	μ_{sq}*
−2.000	80H	−128	

*$\pm \mu_{sq}$ = nominal levels for pure square-wave input
= −1.0 ± 0.25 V = ± 32 units (ADC)